REMARKS/ARGUMENTS

Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Ito et al. (US Patent No. 5,742,782). Claims 1, 7, 8, 12, 13, 19, 20, and 24 have been amended. New claims 25-28 have been added. Applicants respectfully that the claims as amended as well as the new claims are patentable over Ito.

Support for claim amendments and new claims

The specification supports the amendments made to claim 1, 8, 13, and 20. Specifically, the use of multiple-bit data elements to perform arithmetic operations in the manner recited in these claims is described in the specification, for example, at paragraphs [0080], [0213] through [0215], and [0221] through [0225].

The specification supports the amendments made to claims 7, 12, 19, and 24. Specifically, the use of a single instruction to perform multiplication on a plurality of floating-point operands in a first register and a plurality of floating-point operands in a second register in the manner recited in these claims is described in the specification, for example, at paragraphs [0221] through [0223].

The specification supports new claims 25 and 26. The use of an integer arithmetic instruction in the manner recited in claim 25 is described in the specification, for example, at paragraphs [0213] through [0215]. The use of a floating-point arithmetic instruction in the manner recited in claim 26 is described in the specification, for example, at paragraphs [0221] through [0225].

The specification supports new claim 27. The specification discloses a programmable processor as recited in the claim comprising a data path (e.g., paragraphs [0078] and [0079],

describing path connecting registers, memory, and execution units), an external interface (e.g., paragraph [0079], describing external interface 118), a register file (e.g., paragraph [0078], describing register files AR 105-108 and ER 125-128), and an execution unit (e.g., paragraphs [0080] and [0081], describing functional units G143-144 and 146-147 and E141 and 149). The use of a single instruction to perform floating-point arithmetic operations in the manner recited is described in the specification, for example, at paragraphs [0221] through [0225].

The specification supports new claim 28. The specification discloses a data processing system as recited in the claim comprising a bus (e.g., paragraph [0078] and Fig. 1, showing bus connecting microprocessor to external main memory 120, secondary cache memory 119, and I/O devices 120), an external memory (e.g., paragraph [0079] and Fig. 1, showing external main memory 120 and secondary cache memory 119), and a programmable microprocessor (e.g., paragraph [0078] through [0085] and Fig. 1, showing microprocessor within "chip boundary"). The specification further discloses that the microprocessor comprises a data path (e.g., paragraphs [0078] and [0079], describing path connecting registers, memory, and execution units), an external interface (e.g., paragraph [0079], describing external interface 118), a register file (e.g., paragraph [0078], describing register files AR 105-108 and ER 125-128), and an execution unit (e.g., paragraphs [0080] and [0081], describing functional units G143-144 and 146-147 and E141 and 149). The use of a single instruction to perform floating-point arithmetic operations in the manner recited is described in the specification, for example, at paragraphs [0221] through [0225].

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 202-756-8363.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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